REMARKS/ARGUMENTS

After the foregoing amendment, claims 1-24 are currently pending in this application. Paragraph **[0001]** has been amended to update related file information. Claims 1, 4-8, 11-21, and 24 have been amended to more clearly recite inventive subject matter. The amended claims recite or refer to a communications architecture comprising one or more operatively coupled SERDES communication links and novel error correction for use in such an architecture. Support is found at least in Figs. 2-4 and 7, and paragraphs **[0026]**, **[0036]-[0044]**, and **[0056]-[0063]**. No new matter has been introduced into the application by these amendments.

Claim Rejections - 35 USC § 112

Claim 21 and its dependent claim 23 stand rejected under 35 USC § 112 second paragraph as being allegedly indefinite for reciting a variable "n" which is undefined. Claim 21 has been amended to more clearly define "n". Withdrawal of the 35 USC § 112 rejection of these claims is respectfully requested.

Claim Rejections - 35 USC § 102

Claims 12-23 stand rejected under 35 USC § 102(b) as being allegedly anticipated by Benson (U.S. Pat. No. 5,907,566, hereinafter "*Benson*"). Applicant respectfully traverses this rejection.

The claims of the present application are directed to a data communications architecture employing serializers and deserializers communicating over links (SERDES links) for use in communicating data between computer processing components of a computing environment. In exemplary implementations disclosed in the present application and in the claims, one or more

SERDES links are operatively coupled together to provide for high speed, low latency communications, such as for use in a computer infrastructure (see, e.g., paragraph **[0026]**, "the illustrative implementation may orchestrate the use of multiple parallel SERDES communications channels"; Figs. 2-4 showing transmit and receive cores each having one or more serializers and deserializers, respectively, whose operation is orchestrated by logic blocks; and paragraphs **[0036]** *et seq.*) In an illustrative operation, accurate communications across the SERDES links can occur since in an illustrative implementation retry data transfers are allowed to occur. To retry a transmission, an error is first detected. In this context, the data block that is validated is the amount of data that is sent across the multiple links in one encoding cycle, such as in an 8b10b encoding cycle. In the illustrative operation, an error is indicated if the disparity of data received at the receiving end of the operatively coupled links does not match the disparity of the data at the transmitting end. If the disparity of the transmitted data is known at the receiving end, and it does not match the disparity of the received data, an error can be detected immediately. To achieve this result, the disparity of the transmitted data is used to generate an error code at the transmitting end. The error code can then be passed to the receiving end using a separate SERDES channel. The receiving end can generate an error code from the received data, and can compare it to the error code of the transmitted data. If the codes indicate different disparities in the transmitted data and the received data, a transmission error is indicated, and a request to resend the errant data can be issued immediately.

The number of bits of the error code can be selected depending on, for example, the number of links in a group and/or the number of bits in the encoding scheme. Illustratively in an 8b10b encoding scheme, a 5 bit error code can be selected, which can be sufficient to catch single bit errors of a given type, and multi-bit errors as well. A 5 bit to 10 bit encoding can then

be used to send the error code which avoids introducing additional latency in the error detection. Illustratively, each of the 5 bits of the error code is sent twice, once as a positive true and once as a negative true or complement, thereby achieving neutral disparity in the error code transmission, and not adversely affecting system timing.

In contrast, *Benson* discloses a continuous byte-stream encoder/decoder using frequency increase, for use with a byte stream of asynchronous transfer mode (ATM) data cells. The ATM data cells are received with a plurality of words, each word comprising a plurality of bits in parallel. Each data cell is analyzed and control words are created and added to the data words to create a combined data and control word stream. The control words convey information such as start-of-cell, parity and synchronization signals. The combined word stream has a higher word transfer rate than the original ATM data cells. The combined stream is encoded by a known 8B/10B encoder, serialized through a known serializer, and passed over a single serial communication path. At the receiving end, the serial signal is deserialized through a known deserializer, decoded with both an 8B/10B decoder and a frequency decreasing decoder, and the data restored to its original data cell format.

Benson discloses error checking as applied to an individual serial bit stream over a single serial communication path. (See *Benson* column 6 lines 13-31.) However, unlike the claims of the present application, *Benson* does not disclose or suggest that SERDES links be operatively coupled and orchestrated as SERDES communication channels having a transmitting end and a receiving end for data communications. Nor does *Benson* disclose or suggest error checking that can detect errant data such as would be caused in such an arrangement by one of the operatively coupled SERDES links that is not operating properly. Therefore, since *Benson* does not teach all of the elements of claims 12 and 21 of the present application, it does not anticipate claims 12

and 21, and claims 12 and 21 are allowable over *Benson*. Claims 13-20 and 22-23 depend from claims 12 and 21, respectively. Therefore, without prejudice to their individual merits, these claims are also allowable. Hence, withdrawal of the 35 USC § 102(b) rejection of claims 12-23 is respectfully requested.

Claim Rejections - 35 USC § 103

To establish a prima facie case for obviousness under 35 USC § 103(a), it must be shown that the asserted references, when read alone, or in combination, teach all of the elements of the examined claims. Also, a motivation to combine the references must be shown if more than one reference is being asserted.

Claims 1-11 and 24 stand rejected under 35 USC § 103(a) as being allegedly unpatentable over Fredrickson (U.S. Pat. No. 6,154,870, hereinafter "*Fredrickson*") in view of *Benson* (same as above). Applicants believe the Examiner meant this 103 rejection to refer to Ramamurthy et al. (U.S. Pat. No. 5,790,563, hereinafter "*Ramamurthy*") instead of *Benson*, because the § 103(a) arguments refer to *Ramamurthy* and not *Benson*. With this understanding, Applicant respectfully traverses this rejection.

Fredrickson discloses a new Viterbi Partial Response Maximum Likelihood (PRML) error-correction protocol and system. A signal sequence of 8-bit bytes is fed to an encoder that produces 9-bit sequences. These signals are fed to a serializer to produce a precoder input signal, which is fed into a precoder. The precoder outputs a sequence that is transmitted over a medium that is subject to signal degradation caused by noise contamination. A receiver recovers the possibly noisy signal, and feeds it to a Viterbi detector. The detector forms an estimate of the precoder output signal, which is input to an inverse precoder function to yield an estimate of the

precoder input signal. This is fed to a deserializer and deserialized into 9-bit subsequences, which are fed to a decoder to produce an estimate of 8-bit data bytes, as reconstructed to be freed from noise corruption. The resulting output signal is representative of the original signal sequence of 8-bit bytes, despite the imposition of noise corruption during transmission. This arrangement is described to be an example of so-called forward error correction, which allows the receiver to detect and correct errors without the need to ask the sender for additional data. Thus, unlike the present application, no provision is made in *Fredrickson* for retransmission of errant data.

The Examiner asserts that *Fredrickson* calculates a disparity for data being communicated, calculating an error code based on the calculated disparity (citing *Fredrickson* col. 4 line 40 to col. 5 line 3), communicating data between a serializer and a deserializer then calculating a disparity on the received data to generated another error code (citing *Fredrickson* col. 3 lines 3-12). However, these features are not found at the cited locations, nor elsewhere in *Fredrickson*. *Fredrickson* col. 3 lines 3-12 appears to be discussing known usages of so-called convolutional codes, a type of error-correction wherein each m-bit information symbol (here, m=8) is transformed into an n-bit symbol (here, n=9), where m/n is the code rate (here, 8/9), and the transformation is a function of a certain number of adjacent symbols. Such codes have nothing at all to do with the present application.

Fredrickson col. 4 line 40 to col. 5 line 3 describes the generation of these convolutional codes. The code generation of *Fredrickson* does not teach the present application's calculating a disparity for data being communicated by one or more operatively coupled serializers, nor calculating an error code based on the disparity, nor calculating a disparity on the received data

to generate another error code, as recited in independent claims 1, 11, and 24 of the present application.

Because the Examiner relies on *Fredrickson* to teach the limitations of the present application in all 35 USC § 103 rejections, the rejections do not support a *prima facie* case of obviousness under 35 USC § 103(a). Withdrawal of the 35 USC § 103 rejection of claims 1-11 and 24 is respectfully requested.

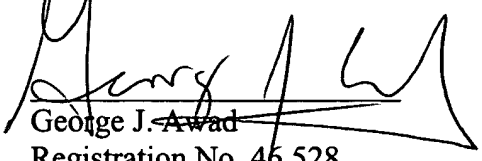
Conclusion

In view of the foregoing amendment and remarks, Applicant respectfully submits that the present application, including claims 1-24, is in condition for allowance and a notice to that effect is respectfully requested.

If the Examiner believes that any additional minor formal matters need to be addressed in order to place this application in condition for allowance, or that a telephone interview will help to materially advance the prosecution of this application, the Examiner is invited to contact the undersigned by telephone at the Examiner's convenience.

Respectfully submitted,

GREGG BERNARD LESARTRE

BY: 

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